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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/840,146	05/06/2004	Helmut Horst Tews	2004 P 51343 US	7404

25962 7590 01/05/2007

SLATER & MATSIL, L.L.P.
17950 PRESTON RD, SUITE 1000
DALLAS, TX 75252-5793

EXAMINER	
RAO, SHRINIVAS H	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/840,146	TEWS ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5 to 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5 to 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

Applicants' amendment filed on October 11, 2006 has been entered and forwarded to the examiner on October17, 2006.

Therefore claims 5 and 6 as amended by the amendment and claims 7-18 as previously recited are currently pending in the Application.

Claims 1 to4 were previously cancelled.

Information Disclosure Statement

No further IDSs after the one filed on May 06, 2005 has been filed in this case.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allison (U.S. Patent .No. 4,047,195 herein after Allison) as previously applied and further in view of Hwang et al. (U.S. Patent No. 4,833,516, herein after Hwang).

With respect to claim 5 Allison describes a single crystal semiconductor structure comprising a trench formed in a single crystal semiconductor body surface (Allison figure 5, co1.3 lines 35-37) said trench having upper sidewall portions perpendicular to and extending from said semiconductor body surface (Hwang figure 3 col. 2 lines 20-35) , said perpendicular sidewalls of the upper portion of the trench disposed in different crystallographic planes,

Allison does not specifically describes said trench having upper sidewall portions perpendicular to and extending from said semiconductor body surface second sidewall portions of said trench a first one of said sidewall portions of thee trench disposed in a first one of different crystallographic planes, said first crystallographic plane perpendicular to said surface a second crystallographic plane, and said second plane also perpendicular to said surface .

However Hwang a patent from the same field of invention describes in figure 4 and col.3 lines 20-42 describes sidewall portions in at least 100 and 110 crystallographic planes and said second plane also perpendicular to said surface to better control the growth of the epitaxial layer to desired thickness which in turn provides a better device made by a simpler process.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Hwang's a second sidewall portions of said trench disposed in a second crystallographic plane and said second plane also perpendicular to said surface in Allison's device. The motivation to make the above combination is to

better control the growth of the epitaxial layer to desired thickness which in turn provides a better device made by a simpler process. (Hwang col.3 lines 10 to 42).

The remaining of limitations of claim 5 :

a first layer of silicon di oxide material grown on said first sidewall potions at a first material and to a first thickness when subjected to a thermal oxidation process, (Allison col. 4 lines 5-10, Hwang col .3 lines 10-2Q). a second layer of silicon dioxide grown on said second sidewall portion at a second rate and on said first layer of said silicon dioxide material at a rate slower than said second rate wherein said first and second sidewall portions of the trench (Allison col.4 lines 30-35, Hwang col.3) are subjected to a thermal oxidation process such that the thickness of said second layer of silicon dioxide on said second sidewall portions is substantially equal lo the thickness of both said first and second layers of silicon dioxide on said first side portions.

The recitation, " (said trench wall having) sidewall portions perpendicular to said surface" is considered new matter for reasons set out above and not given patent able weight.

It is noted that Hwang (the applied secondary reference) in figures 4-12, etc. shows sidewall (plane 100 portion) being perpendicular to said surface.

The recitation, "are subjected to a thermal oxidation process such that the thickness of said second layer of silicon dioxide on said second sidewall portions is substantially equal lo the thickness of both said first and second layers of silicon dioxide on said first side portions." Is taken to be a product by process recitation for which patentable weight cannot be given in the presently recited device claims. See in re

Fessman, 180 U5PQ324,326(CCPA 1974); In re Marosi et al. 218 U5PQ289,292 (Fed. Cir. 1983) and particularly In re Thrope 227 USPQ964, 966 (Fed. Cir. 1985) see also MPEP 2113.

With respect to claim 6 Allison describes a single crystal semiconductor structure comprising: a trench formed in single crystal semiconductor body surface having upper sidewall portions perpendicular to and extending from dais semiconductor body surface said surface and said perpendicular sidewalls of the upper portion of the trench disposed in different crystallographic planes of-said semiconductor body : a relatively thin material formed on selected sidewall portions (Hwang fig.3 etc, Allison 5g.5 #18, col.2 lines 2 65-68, Hwang of said trench residing in a first one of said different crystallographic planes perpendicular perpendicular to said surface, a layer of silicon di oxide grown over said relatively thin material at a first rate by a thermal l oxidation process to a selected thickness, and said silicon dioxide grown at a second rate during said thermal oxidation process on unselected sidewall surface portions of-said trench without said thin material and said unselected sidewalls residing in a second one of said different crystallographic planes that is also perpendicular to said surface, (see rejections under claims land 5 above) said second rate faster than said first rate such that the resulting thickness of said silicon dioxide grown over both the selected sidewall portions and the unselected sidewall portions is substantially uniform (Allison co1.4 lines 30-35, figures 5,8- Hwang fig. 4, etc.)

With respect to claim 7 Allison describes a semiconductor body of claim 5 wherein said first sidewall portions are disposed in the <1 10> crystallographic plane and said second sidewall portions are disposed in the <100> crystallographic plane. (Hwang figure 4, etc.)

With respect to claim 8 Allison describes the semiconductor body of claim 6 wherein the relatively thin material is silicon nitride. (well known in the ad e.g. Haung reference in Applicants' IDS).

With respect to claim 9 Allison describes the semiconductor body of claim 6 further comprising another layer of silicon di oxide formed on said relatively thin material such that said another layer of silicon dioxide and said layer of silicon dioxide grown over said relatively thin material have a combined thickness substantially the same as the thickness of said layer of silicon dioxide grown on said unselected surface portions of said semiconductor body. (rejected for reasons set out under claim 5 above).

With respect to claim 10 Allison describes the semiconductor body of claim 6 wherein the relatively thin material is less than 20 angstroms. (Allison co1.4 lines 30-43).

With respect to claim 11 Allison describes the semiconductor body of claim 6 wherein the relatively thin material forms a layer which is thinner than the corresponding oxide layer grown on the selected and unselected surface portions. (Allison col.4 lines 30-35, figures 5-8- equal thickness on side walls).

With respect to claim 12 Allison describes the semiconductor body of claim 6 wherein said first sidewall portions are dispersed in the <110> crystallographic plane

and said second sidewall portions are disposed in the <100> crystallographic plane. (Hwang figure 4 ,etc.)

With respect to claims 13 to 15 Allison describes the semiconductor body of claims 1,5 and 6 wherein said trench is oval shaped. (Allison figures, Hwang figs,)

With respect to claims 16 and 18 Allison describes the semiconductor body of claim 1 wherein said trench comprises a capacitor in a lower portion and a FET in an upper portion to form a DRAM cell. (Hwang col. line 20, line 30-31, col.2 lines 23-25).

With respect to claim 17 Allison describes the semiconductor body of claim 5 wherein said trench comprises a capacitor in a lower portion and a FET in an upper portion to form a DRAM cell.(Allison figures Hwang figs. 1, 12 and co1.2 lines 23-25).

Response to Arguments

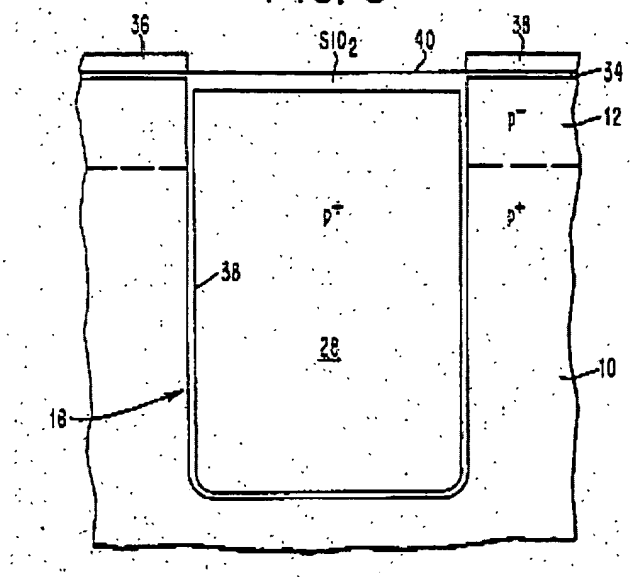
Applicant's arguments filed March 23, 2006 and April 24, 2006 have been fully considered but they are not persuasive for set out at length above and incorporated here by reference.

Applicants' first argument that the applied Allison reference does not show sidewall portions of the Allison trench are perpendicular to the surface of the semiconductor body is not persuasive because :

Applicants' contention the Allison and Hwang does disclose :

A) a first upper sidewall portion in a first crystallographic plane perpendicular to the semiconductor body is not persuasive as Hwang in fig.3 describes this limitation (figure 3 reproduced below).

FIG. 3



Similar if not identical to Applicants' figures.

B) Applicants' second contention that Allison and Hwang do not disclose a second upper sidewall portion in a second crystallographic plane is not persuasive because Allison col. 4 lines 1-5, and Hwang col.3 disclose this limitation.

Allison col. 4 lines 30-35 states :

which are oriented in a crystal plane which is different from the <100> plane and, as shown in FIG. 3, are in the <111> crystal plane with the planar bottom walls 17 being oriented in the 100 crystal plane parallel to the surface of the epitaxial layer 13.

Therefore all of Applicants' contention are not persuasive.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571)272-1718. The examiner can normally be reached on 8.00 to 5.00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fahmy Wael can be reached on (571) 272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven H. Rao

Patent Examiner

December 19, 2006.

HOWARD WEISS
PRIMARY EXAMINER